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1 Introduction

This document describes how to construct a radio power table for devices supporting version 2.0 + EDR of the Bluetooth® wireless technology specification, and how to upload the power table into the Persistent Store (PS) database.

The primary focus of this document is enhanced radio power table construction for firmware builds Unified21a and later. Section 2 describes power table construction for Class 2 and Class 3 designs, while section 3 describes the additional configuration settings that are required when completing a Class 1 design.

The power table functionality for firmware build HCIStack2.0EDRv19.2 (the first build to support version 2.0 + EDR of the Bluetooth specification) differs slightly. Changes to the enhanced power table that are required if constructing a power table for use with HCIStack2.0EDRv19.2 are described in section 4.

Section 5 provides a summary of PS keys that are related to the enhanced radio power table and that may need to be configured for each design.

Power table construction must be done once for each new Bluetooth design. The Persistent Store values become part of the set downloaded to every instance of a design at manufacture (for flash-based parts in typical usage scenarios) or at run-time (typically for ROM-based parts). It is not generally necessary to construct a unique power table for every instance of a design, unless factors external to BlueCore can cause significant variability in power output. The default values provided in CSR firmware power tables may suit the modules in the Casira CSR development toolkit. It is unlikely that they will be appropriate for customer designs and should therefore be modified.

For information on power table construction for firmware builds that do not use EDR, refer to the Power Table Construction application note.
2 Class 2 and Class 3 Enhanced Radio Power Table

2.1 Enhanced Power Table Overview

The enhanced radio power table, configured using PSKEY_LC_ENHANCED_POWER_TABLE, is used by BlueCore to implement transmit power control in devices supporting version 2.0 + EDR of the Bluetooth specification. Devices using firmware with EDR support must use this power table, whereas devices using firmware supporting only Basic Rate operation (HCIStack1.2v18.x and earlier) must continue to use the Basic Rate power table, configured using PSKEY_LC_POWER_TABLE. The two tables are mutually exclusive. For details on constructing the Basic Rate power table, refer to the Power Table Construction application note. For details on transmit power control in BlueCore, refer to the Transmit Power Control application note.

The transmission path in a typical BlueCore design contains several amplifiers, both internal to the chip and (if required) external to the chip. The enhanced radio power table provides a mapping between the amplifier gain settings for both Basic Rate and EDR modes of operation and transmit power. The table is structured as an ordered set of rows, where the values in each row contain both Basic Rate and EDR amplifier settings required to produce a particular output power level (specified in dBm).

The Link Manager responds to peer requests to increase and/or decrease transmit power by stepping up or down rows in the power table. Internal and (if applicable) external PA settings are then set to their new values, affecting the output power accordingly. The output power value is read by both internal device functions and higher layers using the HCI command Read_Transmit_Power_Level. It is therefore important that the transmit power levels are accurately correlated with their corresponding amplifier settings.

The Bluetooth specification only requires devices operating above +4dBm (i.e. Class 1 devices) to implement transmit power control. Power tables for Class 2 and Class 3 devices could be limited to a single entry that meets the corresponding Bluetooth transmit power specification (which would restrict those devices to transmissions at that single power level only). This is not, however, recommended by CSR.

Lower power settings can improve the performance of devices that are very close together. They can also serve to reduce collisions between piconets, giving improved performance in crowded environments. CSR strongly recommends that all devices have a power table that extends down to at least -20dBm.

2.2 Power Table Parameters

The enhanced power table contains the amplifier settings for both Basic Rate and EDR transmissions and the corresponding transmit power level. In addition, the power table contains two control bits that can be used to increase configuration options within a design.

If EDR support in the firmware is disabled (using PSKEY_LOCAL_SUPPORTED_FEATURES, described in section 5.4), then the EDR settings within the enhanced power table are ignored. The Basic Rate parameters must still be configured for correct Basic Rate operation.

Each row in the enhanced radio power table contains the following parameters:

- Basic Rate internal PA (INT PA) gain setting
- Basic Rate external PA (EXT PA) gain setting
- External PA (EXT PA) control bit
- EDR internal PA (INT PA) gain setting
- EDR external PA (EXT PA) gain setting
- EDR TX pre-amplifier (TX-PRE) gain setting
- TX_PA_ATTEN\(^1\) setting
- EDR control bit

\(^1\)BlueCore4-Audio ROM and BlueCore4-Audio Flash only
### 2.2.1 Basic Rate INT PA Gain

The Basic Rate INT PA gain setting controls BlueCore’s internal power amplifier during Basic Rate operation. The internal PA has a 6-bit control and so can be adjusted from 0 (0x00) to 63 (0x3f). For Class 2 and 3 devices, the internal PA is used to provide power control within a Basic Rate link.

### 2.2.2 EXT PA Gain and EXT PA Control Bit

The EXT PA gain setting (for both Basic Rate and EDR) and the EXT PA control bit setting are only used in Class 1 devices operating with an external PA. Details on these parameters are provided in section 3.1. For Class 2 and Class 3 designs not using an external PA, these parameters should be set to 0.

### 2.2.3 EDR INT PA Gain

The EDR INT PA gain setting controls BlueCore’s internal PA during EDR operation. For Class 2 and 3 devices, the EDR INT PA gain is typically set to a constant value of 63 (0x3f).

### 2.2.4 EDR TX-PRE Gain

BlueCore has an internal pre-amplifier (TX-PRE) that is used for gain control with EDR transmissions. The pre-amplifier gain setting in the power table can be adjusted from 60 (0x3c) to 105 (0x69).

For Basic Rate transmissions, TX-PRE is set to a fixed value defined by PSKEY_TX_PRE_LEVEL. This should not be changed from its default setting unless advised by CSR.

### 2.2.5 TX_PA_ATTEN

The TX_PA_ATTEN parameter is used on BlueCore4-Audio ROM and BlueCore4-Audio Flash chips (in conjunction with TX-PRE) to adjust EDR output power. Refer to Section 2.4.2 for more details.

### 2.2.6 EDR Control Bit

The EDR control bit indicates power settings that are unavailable for EDR transmissions. Different maximum power limits can be set for Basic Rate and EDR transmissions by setting the EDR control bit to 1 in all power table entries exceeding the maximum EDR transmit power setting.

The EDR control bit is more commonly used with Class 1 designs. However, for some Class 2 designs the maximum transmit power for EDR transmissions may be slightly lower than the maximum transmit power for Basic Rate transmissions. This may require the EDR maximum power limit to be set to one entry below the Basic Rate power limit.

Lower power Class 3 designs should have identical values for maximum EDR and Basic Rate power. The EDR control bit should therefore be set to 0 for all entries.

BCCMD command LIMIT_EDR_POWER defines how the firmware deals with transmissions that have the corresponding EDR control bit set. If LIMIT_EDR_POWER is disabled (the default), then EDR transmissions with the EDR control bit set are renegotiated to Basic Rate. Alternatively, if LIMIT_EDR_POWER is enabled, then the firmware limits transmit power in the link to the maximum entry containing an EDR control bit value of 0.

### 2.2.7 Transmit Power Level

The power table’s maximum transmit power must not exceed the transmit power limits for that class of device:

- 0 to +20dBm for Class 1 devices
- -6dBm to +4dBm for Class 2 devices
- Equal to or less than 0dBm for Class 3 devices
CSR recommends the minimum transmit power entry be below -20dBm to minimize interference in crowded environments and improve communications between closely located devices, as described in section 2.1. The step size between consecutive entries in the power table is required to be greater than 2dB and less than 8dB to meet the Bluetooth specification requirements for transmit power control. CSR recommends using step sizes of around 4dB.

2.3 Measuring Output Power

Transmit power and the corresponding amplifier settings can be readily computed using CSR’s BlueTest and a spectrum analyzer. BlueTest and spectrum analyzer settings required to compute both Basic Rate and EDR measurements are given in the next section. Alternatively, commercial Bluetooth testers can be used to conduct the power measurements, if available.

2.3.1 Basic Rate Measurement Procedure

Using CSR’s BlueTest, BlueCore can be configured to transmit a PRBS9 DH5 packet at 2441MHz. The BlueTest settings are given in Table 2.1.

<table>
<thead>
<tr>
<th>TXDATA1</th>
<th>CFG_FREQ</th>
<th>CFG_PKT</th>
</tr>
</thead>
<tbody>
<tr>
<td>LO_Freq</td>
<td>Ext_Pow</td>
<td>Int_Pow</td>
</tr>
<tr>
<td>2441</td>
<td>EXT PA</td>
<td>INT PA</td>
</tr>
<tr>
<td></td>
<td>level</td>
<td>level</td>
</tr>
<tr>
<td></td>
<td>(e.g. 0)</td>
<td>(e.g. 63)</td>
</tr>
<tr>
<td>TXRX_Int</td>
<td>12500</td>
<td>1875</td>
</tr>
<tr>
<td>Loopback_Int</td>
<td>1</td>
<td>15</td>
</tr>
<tr>
<td>Report_Int</td>
<td>339</td>
<td></td>
</tr>
<tr>
<td>Pkt_Type</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pkt_Size</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 2.1: BlueTest Settings for PRBS9 DH5 Packet Transmission

Ext_Pow and Int_Pow correspond to the Basic Rate EXT PA and Basic Rate INT PA power table settings.

The average output power across a packet can be monitored on a spectrum analyser set up as shown in Table 2.2.

<table>
<thead>
<tr>
<th>Span</th>
<th>Sweep</th>
<th>RBW/VBW</th>
<th>Y Axis</th>
<th>Trigger</th>
<th>Trigger Offset</th>
<th>Detector Mode</th>
<th>Average Type</th>
<th>Average</th>
</tr>
</thead>
<tbody>
<tr>
<td>0MHz</td>
<td>5ms</td>
<td>3MHz</td>
<td>10dB/div</td>
<td>Video</td>
<td>-1ms</td>
<td>Sample</td>
<td>Power (RMS)</td>
<td>ON</td>
</tr>
</tbody>
</table>

Table 2.2: Spectrum Analyser Settings for Transmit Power Measurements

An example of the expected output is shown in Figure 2.1.
For Class 2 and 3 devices, power control during Basic Rate operation is provided by varying the INT PA setting. The EXT PA setting is ignored because the device is not configured for operation with an external PA.

Record the amplifier settings for each desired transmit power entry in the table. These are entered later into PSKEY_LC_ENHANCED_POWER_TABLE.

### 2.3.2 Enhanced Data Rate Measurement Procedure

DQPSK 2-DH5 and 8DPSK 3-DH5 packets with PRBS9 payloads can be transmitted in BlueTest using the settings given in Table 2.3 and Table 2.4.

<table>
<thead>
<tr>
<th>TXDATA1</th>
<th>CFG_FREQ</th>
<th>CFG_PKT</th>
</tr>
</thead>
<tbody>
<tr>
<td>LO_Freq</td>
<td>Ext_Pow</td>
<td>Int_Pow</td>
</tr>
<tr>
<td>2441</td>
<td>EXT PA level (e.g. 0)</td>
<td>TX-PRE level (e.g. 105)</td>
</tr>
</tbody>
</table>

Table 2.3: BlueTest Settings for PRBS9 2-DH5 Packet Transmissions
Table 2.4: BlueTest Settings for PRBS9 3-DH5 Packet Transmissions

When transmitting EDR packets using BlueTest or radio test mode, Int_Pow controls the chip's pre-amplifier (TX-PRE) gain. The first entry in the power table is now used to determine the fixed internal PA setting for EDR operation.

Notes:

It is very important that the first row of PSKEY_LC_ENHANCED_POWER_TABLE (i.e. the entry corresponding to minimum transmit power) is configured with the correct EDR INT PA setting before conducting any EDR power measurements. Most designs should use a fixed EDR INT PA setting of \[ 63 \]

On BlueCore4-Audio ROM and BlueCore4-Audio Flash chips the value of the TX_PA_ATTEN parameter in radio test mode comes from the last entry in the power table. This is not currently configurable from BlueTest.

Average power can be measured on a spectrum analyzer using the settings given in Table 2.5.

Table 2.5: Spectrum Analyser Settings for EDR Transmit Power Measurements

In configuring the measurement, the trigger level should be set before enabling the averaging function. If the trigger amplitude is set too low, then the spectrum analyser can falsely trigger off of the noise floor. Conversely, if the trigger amplitude is set too high, then dips in transmit power during the packet can cause the spectrum analyser to retrigger.

An example of the expected output is shown in Figure 2.2.
EDR packets contain GFSK modulation through the packet header and higher-order DPSK modulation through the packet payload. EDR average power measurements are based upon the average power as measured across the DPSK payload.

### 2.4 Adjusting EDR Output Power

EDR power control on early BlueCore4 chips (BlueCore4-External and BlueCore4-ROM) is achieved by varying the TX_PRE level with INT_PA set to 63. The BlueCore4-Audio ROM and BlueCore4-Audio Flash chips have an additional TX_PA_ATTEN parameter which allows some of the output stage transistors to be turned off for lower EDR output powers, thereby using less current.

#### 2.4.1 BlueCore4-External and BlueCore4-ROM

Output power is changed by varying the TX-PRE gain. As with Basic Rate transmissions, the EXT PA setting is ignored.

Adjust TX-PRE level to obtain the desired transmit power levels and record the corresponding amplifier settings. This information must be entered into PSKEY_LC_ENHANCED_POWER_TABLE.

#### 2.4.2 BlueCore4-Audio ROM and BlueCore4-Audio Flash

EDR power control on BlueCore4-Audio ROM and BlueCore4-Audio Flash is achieved using a combination of TX_PRE and TX_PA_ATTEN. Start with TX_PA_ATTEN set at 0 for maximum power, and increase by one for each power step, adjusting TX_PRE to give the required output power.

If more than eight power steps are required, leave TX_PA_ATTEN at 7 and continue to decrease the TX_PRE level.
2.5 Committing Power Table to Persistent Store

The enhanced radio power table is stored in Persistent Store under the PS key PSKEY_LC_ENHANCED_POWER_TABLE. Any values set in PSKEY_LC_POWER_TABLE are ignored by firmware supporting EDR operation.

The data can be entered in two different formats:

- Tabular form using PSTool
- Raw data using BTCli, BlueTest or PSTool

Note:

If PSKEY_LC_ENHANCED_POWER_TABLE is not listed in the default key settings in PSTool, then the data must be entered in raw data form using the utility’s “Edit Raw” command. Both formats are described in the next section.

2.5.1 PSTool Method

The most user-friendly way of entering data into the power table is to use PSTool, which allows the decimal information to be entered in a simple table format. Rows in the table can be inserted or deleted as required.

Figures differ depending on the chip:

- BlueCore4-External and BlueCore4-ROM
- BlueCore4-Audio ROM and BlueCore4-Audio Flash

Table 2.6 shows an example of the enhanced radio power table for a Class 2 device using BlueCore4-External or BlueCore4-ROM as displayed in PSTool.

<table>
<thead>
<tr>
<th>Basic Rate Amplifier Settings</th>
<th>Control Bit</th>
<th>Enhanced Data Rate Amplifier Settings</th>
<th>Control Bit</th>
<th>Output Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>INT PA</td>
<td>EXT PA</td>
<td>EXT PA</td>
<td>INT PA</td>
<td>EXT PA</td>
</tr>
<tr>
<td>7</td>
<td>0</td>
<td>0</td>
<td>63</td>
<td>0</td>
</tr>
<tr>
<td>13</td>
<td>0</td>
<td>0</td>
<td>63</td>
<td>0</td>
</tr>
<tr>
<td>20</td>
<td>0</td>
<td>0</td>
<td>63</td>
<td>0</td>
</tr>
<tr>
<td>28</td>
<td>0</td>
<td>0</td>
<td>63</td>
<td>0</td>
</tr>
<tr>
<td>36</td>
<td>0</td>
<td>0</td>
<td>63</td>
<td>0</td>
</tr>
<tr>
<td>44</td>
<td>0</td>
<td>0</td>
<td>63</td>
<td>0</td>
</tr>
<tr>
<td>53</td>
<td>0</td>
<td>0</td>
<td>63</td>
<td>0</td>
</tr>
<tr>
<td>63</td>
<td>0</td>
<td>0</td>
<td>63</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 2.6: Enhanced Radio Power Table Settings for BlueCore4-External/ROM

Notes:

- Power table entries must be specified in ascending order of transmit power.
- Newer versions of PSTool will display the TX_PA_ATTEN parameter (as used with BlueCore4-Audio ROM and BlueCore4-Audio Flash) with 0 values. This can be ignored.
Table 2.7 shows an example of the enhanced radio power table for a Class 2 device using BlueCore4-Audio ROM or BlueCore4-Audio Flash as displayed in PSTool.

![Table 2.7: Enhanced Radio Power Table Settings for BlueCore4-Audio ROM/Flash](image)

**Note:**

Power table entries *must* be specified in ascending order of transmit power.

### 2.5.2 Raw Data Method

It is possible to enter the raw hexadecimal data into the Persistent Store using PSTool’s “Edit Raw” facility, BlueTest or BTCli.

The PS database stores the power table as an ordered array of “power_setting” types. Each array element of type “power_setting” holds eight bytes within five uint16s and represents the configuration for one particular transmit power.

The Class 2 power table shown in Table 2.6 (for BlueCore4-External and BlueCore4-ROM) has the following hexadecimal data structure:

```
0700 0000 3f00 4400 e700
0d00 0000 3f00 4600 eb00
1400 0000 3f00 4b00 ef00
1c00 0000 3f00 4f00 f300
2400 0000 3f00 5200 f700
2c00 0000 3f00 5800 fb00
3500 0000 3f00 6000 ff00
3f00 0000 3f00 6900 0300
```
The Class 2 power table shown in Table 2.7 (for BlueCore4-Audio ROM and BlueCore4-Audio Flash) has the following hexadecimal data structure:

```
0700 0000 3f00 5a70 e700
0d00 0000 3f00 5760 eb00
1400 0000 3f00 5850 ef00
1c00 0000 3f00 5840 f300
2400 0000 3f00 5a30 f700
2c00 0000 3f00 5c20 fb00
3500 0000 3f00 6010 ff00
3f00 0000 3f00 6900 0300
```

The first five 16-bit words in the data structure for BlueCore4-External and BlueCore4-ROM correspond to the first row in Table 2.6. Splitting into the different power table parameters gives the values in Table 2.8.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Dec Value</th>
<th>Hex Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Basic Rate internal PA</td>
<td>7</td>
<td>0x07</td>
<td>Most significant byte of first uint16</td>
</tr>
<tr>
<td>Basic Rate external PA</td>
<td>0</td>
<td>0x00</td>
<td>Least significant byte of first uint16</td>
</tr>
<tr>
<td>External PA control bit</td>
<td>0</td>
<td>0x00</td>
<td>Least significant bit of second uint16</td>
</tr>
<tr>
<td>EDR internal PA</td>
<td>63</td>
<td>0x3f</td>
<td>Most significant byte of third uint16</td>
</tr>
<tr>
<td>EDR external PA gain</td>
<td>0</td>
<td>0x00</td>
<td>Least significant byte of third uint16</td>
</tr>
<tr>
<td>EDR TX pre-amplifier gain</td>
<td>68</td>
<td>0x44</td>
<td>Most significant byte of fourth uint16</td>
</tr>
<tr>
<td>TX_PA_ATTEN(^2)</td>
<td>0</td>
<td>0x00</td>
<td>Most significant nibble of least significant byte of fourth uint16</td>
</tr>
<tr>
<td>EDR control bit</td>
<td>0</td>
<td>0xe7</td>
<td>Least significant bit of fourth uint16</td>
</tr>
<tr>
<td>Transmit power level (dBm)</td>
<td>-25</td>
<td>0xe7</td>
<td>Most significant byte of fifth uint16</td>
</tr>
</tbody>
</table>

Table 2.8: Power Table Parameters

The most significant byte in the second and the least significant byte in the word should be set to 0. Output power follows a 2's complement format.

\(^2\) BlueCore4-Audio ROM and BlueCore4-Audio Flash only.
3 Class 1 Enhanced Radio Power Table

This section explains how to configure an enhanced radio power table for Class 1 designs. Standard Class 1 designs using either a fixed-gain or variable-gain external PA are possible. Support is also provided for dynamic switching of an external PA.

3.1 Class 1 Power Table Parameters

In addition to the power table parameters that are configured for Class 2 and Class 3 operation, the external PA gain settings and control bits must be set for Class 1 operation.

3.1.1 EXT PA Gain

An 8-bit voltage DAC (AUX_DAC) is used to control the amplification level of the external PA for Class 1 operation. The AUX_DAC voltage is set by the corresponding Basic Rate (EDR) EXT PA gain control setting during Basic Rate (EDR) operation if PSKEY_TXRX_PIO_CONTROL has the AUX_DAC configured for gain control of an external PA. If not, then the EXT PA gain settings are ignored.

The output voltage of the AUX_DAC is given by:

\[
V_{DAC} = \min\left(3.3V \times \frac{\text{EXT_PA_GAIN}}{255}, (VDD\_PIO - 0.3V)\right)
\]

for a load current \(\leq 10\text{mA}\) sourced from BlueCore, or

\[
V_{DAC} = \min\left(3.3V \times \frac{\text{EXT_PA_GAIN}}{255}, (VDD\_PIO)\right)
\]

for no load current. It is set from an 8-bit register with the two least significant bits ignored, giving 64 control levels ranging from \(0\) (\(0x00\)) to \(255\) (\(0xff\)), with a step size of 4.

Table 3.1 gives a summary of the different transmit gain control options that can be used with an external PA in a Class 1 designs.

<table>
<thead>
<tr>
<th>Device Behaviour</th>
<th>Basic Rate/EDR EXT PA Setting</th>
<th>PSKEY_TXRX_PIO_CONTROL(^\text{C})</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fixed-gain External PA</td>
<td>AUX_DAC is disabled, EX PA gain settings are ignored</td>
<td>Set to 1, 3 or 5 (depending on RF front-end configuration)</td>
</tr>
<tr>
<td>Variable-gain External PA</td>
<td>AUX_DAC gain given by corresponding EX PA gain setting</td>
<td>Set to 2 or 4 (depending on RF front-end configuration)</td>
</tr>
</tbody>
</table>

Table 3.1: Configuration Options for Transmit Gain Control and Power Ramping

3.1.2 EXT PA Control Bit

The EXT PA control bit is used to enable dynamic switching of an external PA. If the EXT PA control bit is enabled in any of the power table entries, then dynamic switching of an external PA is assumed: the EXT PA control bit is disabled for low-power entries that do not use an external PA, but the EXT PA control bit is enabled for high-power entries that use an external PA.

Low-power transmissions (EXT PA control bit set to 0) assert the PIO defined in PSKEY_TX_AVOID_PA_CLASS1_PIO. This can be used as a control signal for external switches to bypass the external PA. If PSKEY_TXRX_PIO_CONTROL is configured to pull PIO[1] high during TX (typically used to enable an external PA), then this is overridden and PIO[1] is pulled low.

\(^\text{C}\) Refer to section 5 for details on the different PSKEY_TXRX_PIO_CONTROL settings.
High-power transmissions (EXT PA control bit set to 1) will de-assert the PIO defined in PSKEY_TX_AVOID_CLASS1_PIO. PIO[1] will be pulled high during TX if it is configured in PSKEY_TXRX_PIO_CONTROL.

If no entries in the power table have the EXT PA control bit set, then PSKEY_TX_AVOID_PA_CLASS1_PIO is ignored and the PSKEY_TXRX_PIO_CONTROL control setting is directly applied.

Designs using a switchable external PA must be configurable for both Class 2 and Class 1 operation. Standard PS keys should be set for Class 2 operation, while Class 1 parameters are set in Class 1-specific keys. For transmissions with the EXT PA control bit enabled, Class 1 logic is enabled and the Class 1-specific PS keys override normal device operating parameters. For example, PSKEY_TRANSMIT_OFFSET_CLASS1 and PSKEY_TX_PRE_LVL_CLASS1 override settings in PSKEY_TRANSMIT_OFFSET_HALF_MHZ (PSKEY_TRANSMIT_OFFSET if set) and PSKEY_TX_PRE_LVL. The PS key documentation available with each firmware build describes all Class 1-specific keys that are available with that firmware build.

Dynamic switching of an external PA is supported in radio test mode (including BlueTest) if the power table contains a non-zero EXT PA control bit in any of its entries. If a test is then executed with a non-zero EXT PA gain setting, Class 1 logic is assumed: Class 1-specific PS keys settings are used and PIO[1] operation is defined by PSKEY_TXRX_PIO_CONTROL. If a test is executed with an EXT PA gain setting of 0, then low-power operation is assumed: normal device settings are used, PIO[1] is pulled low and the PIO defined by PSKEY_TX_AVOID_PA_CLASS1_PIO is pulled high.

Table 3.2 gives a summary of how to implement Class 1 designs using fixed or dynamic switching of an external PA.

<table>
<thead>
<tr>
<th>Device Behaviour</th>
<th>EXT PA Control Bit</th>
<th>PSKEY_TX_AVOID_PA_CLASS1_PIO</th>
<th>PSKEY_TXRX_PIO_CONTROL</th>
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</thead>
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<tr>
<td>Fixed External PA</td>
<td>Set to 0 in all power table entries</td>
<td>Disabled</td>
<td>Default behaviour</td>
</tr>
<tr>
<td>Switchable External PA</td>
<td>Set to 0 for low-power entries&lt;br&gt;Set to 1 for high-power entries</td>
<td>Set to PIO used as control signal for external switch&lt;br&gt;PIO pulled high for low-power transmissions&lt;br&gt;PIO pulled low for high-power transmissions</td>
<td>PIO[1] pulled low for low-power transmissions&lt;br&gt;PIO[1] pulled high for high-power transmissions</td>
</tr>
</tbody>
</table>

Table 3.2: Configuration Options for External PA

### 3.1.3 EDR Control Bit

As described in section 2.2, the EDR control bit can be used in Class 1 designs to limit power for EDR transmissions. The EDR control bit defines power levels for which EDR transmissions are disallowed. Actual firmware behaviour is defined in conjunction with the BCCMD command EDR_LIMIT_POWER.

If EDR_LIMIT_POWER is disabled (default status), then transmit power settings with the corresponding EDR control bit set are renegotiated to Basic Rate.

If EDR_LIMIT_POWER is enabled, the device refuses to increase transmit power within an EDR link to entries with the control bit set. If PSKEY_LC_DEFAULT_TX_POWER is greater than the maximum allowed EDR power, then the initial link uses Basic Rate. BlueCore can change to EDR once the peer requests it to decrement its power to a transmit power level for which EDR transmissions are allowed.

Table 3.3 shows the different options available for limiting EDR transmit power within a link.
3.2 Class 1 Configuration Options

This section describes design considerations for different types of Class 1 designs.

3.2.1 Gain Control

Gain control in Class 1 designs is normally provided by varying the INT PA settings during Basic Rate operation and EDR TX-PRE gain settings during EDR operation.

For designs that use an external PA for gain control, the internal amplifier levels (i.e. INT PA and TX-PRE) can be held constant and gain control can be provided solely by varying the EXT PA settings.

If using a switchable external PA, then power ramping and gain control should be provided by the internal amplifiers.

3.2.2 Switchable External PA

The presence of both zero and non-zero EXT PA control bits in the enhanced radio power table configures BlueCore for Class 1 operation with a switchable PA. A switchable external PA can allow a device to use an external PA when higher transmit power is required on a link (e.g. above +4dBm) and bypass the PA when lower power is required (e.g. below +4dBm), thereby reducing its power consumption.

An example of how dynamic switching of an external PA can be implemented is shown in Figure 3.1.

![Figure 3.1: Dynamic Switching with External PA](image)

Note:

Alternative configurations for dynamic switching of an external PA are possible, and the selected architecture should be a function of the specific design requirements. Contact CSR Technical Support if additional information is required.
In this example, PIO[1] is used to enable the PA and to connect the PA to the transmit path during high-power operation, while PIO[0] is used to circumvent the PA for low-power operation. PIO[1] and PIO[0] are also used to switch the antenna between transmit (TX) and receive (RX) mode, as required. This mode of operation can be configured using the following Persistent Store settings:

- **PSKEY\_LC\_ENHANCED\_POWER\_TABLE** EXT PA control bit is set to 1 for high-power transmissions (e.g. transmissions above +4dBm) and set to 0 for low-power transmissions (e.g. transmissions below +4dBm).
- **PSKEY\_TX\_AVOID\_PA\_CLASS1** PIO is set to 0, which drives PIO[0] high during low-power transmissions (i.e. transmissions for which the EXT PA control bit is disabled). Signalling on PIO[0] is then used to control the external switches and bypass the external PA during low-power operation.
- **PSKEY\_TXRX\_PIO\_CONTROL** is set to 1 (or 5 depending upon LNA requirements). PIO[1] is driven high for high-power transmissions and low for low-power transmissions. It is used to enable and disable the PA, and as a control signal for the switch, connecting the PA to the TX path during high-power operation. PIO[0] is driven high during low-power transmissions and during RX. It is used as a control signal for the switch, bypassing the PA during lower power transmissions and RX. Setting **PSKEY\_TXRX\_PIO\_CONTROL** to a setting of 2 or 4 allows the AUX\_DAC to be used for gain control of the external PA (if required).

### 3.2.3 Limiting EDR Power

Many of the external power amplifiers currently available have non-linearities that would cause a design using these amplifiers to fail EDR RF qualification at higher power levels. For these designs, EDR transmit power should be limited to the highest transmit power level at which EDR RF qualification is obtained.

The firmware provides a couple of techniques to limit high-power EDR transmissions. For some applications, the most appropriate action may be to drop an EDR link back to Basic Rate operation to maintain connectivity of the link at the required power level. For other applications, a high bandwidth EDR link may be required, in which case it is better to maintain EDR operation without the PA and to risk the link being dropped. CSR EDR firmware allows the system designer to configure the high-power versus high bandwidth trade-off on a per-link basis through the use of the EDR control bit and BCCMD command LIMIT\_EDR\_POWER.

The default method used by the firmware is to renegotiate an EDR link back to Basic Rate packets at the point at which the LMP power control mechanism requests a switch to a higher power level that has the corresponding EDR control bit set to 1. On a return to a lower power setting (i.e. an entry with the corresponding EDR control bit set to 0), a resumption of EDR operation is negotiated if possible. This behaviour therefore makes a best effort to maintain link connectivity at the expense of bandwidth.

Alternatively, the system designer may choose to override the standard LMP power control behaviour and instruct the firmware to limit maximum transmit power within an EDR link. This non-default behaviour is set using LIMIT\_EDR\_POWER, which can be sent from the host to configure this behaviour on a per-link basis. EDR power is restricted to the maximum level configured for EDR transmissions in **PSKEY\_LC\_ENHANCED\_POWER\_TABLE** (i.e. an entry with the corresponding EDR control bit set to 0). If **PSKEY\_LC\_DEFAULT\_TX\_POWER** is greater than the maximum allowed EDR power, then the initial connection is restricted to Basic Rate packets. BlueCore switches to EDR when the peer requests it to decrement its power to a transmit power level for which EDR transmissions are allowed, after which the maximum power within the EDR link is capped.

In the LMP power control mechanism, a receiver sends power up (down) messages to a peer device to try and keep received power within a Golden Receive Power Range (the range in which receiver operation is most efficient). The peer device then attempts to increase (or decrease) transmit power in response to these LMP power control messages. The lower limit of the Golden Receive Power Range is typically several dB higher than the device’s actual receive sensitivity (behaviour that also helps protect against in-band fading caused by multipath, etc.) and hence the switch to a higher power typically occurs sooner than absolutely necessary.

Overriding the standard LMP power control behaviour using BCCMD command LIMIT\_EDR\_POWER would prevent the switch to Basic Rate operation when the bottom of the receiver’s Golden Receive Power Range is reached. This effectively increases the dynamic range for an EDR link (e.g. increasing the operating range for the EDR link), but runs the risk of potential link loss if there is a large decrease in receive power (e.g. if the distance between the devices increases significantly).
4 Power Table Construction for HCIStack2.0EDRv19.2

The functionality for both EDR and EXT PA control bits changed between firmware build HCIStack2.0EDRv19.2 and later builds (Unified21a and later). Differences in power table construction between HCIStack2.0EDRv19.2 and later builds are described in this section and must be taken into account if configuring a power table with HCIStack2.0EDRv19.2.

4.1 Class 2 and Class 3 Power Table Configuration

HCIStack2.0EDRv19.2 supports version 2.0 + EDR of the Bluetooth specification, and hence it uses the enhanced radio power table given by PSKEY_LC_ENHANCED_POWER_TABLE. The power table structure is unchanged from later firmware builds. Power table parameters are:

- Basic Rate INT PA gain setting
- Basic Rate EXT PA gain setting
- EXT PA control bit
- EDR INT PA gain setting
- EDR EXT PA gain setting
- EDR TX-PRE gain setting
- EDR control bit
- Transmit power level (dBm)

Class 2 and Class 3 power table construction follows the same procedure as described in section 2; Basic Rate INT PA, EDR INT PA and EDR TX-PRE gain settings are computed for different output power levels and then entered into the power table. The EXT PA gain and EXT PA control bit settings are set to 0 for all power table entries.

In HCIStack2.0EDRv19.2, the EDR control bit is not used for limiting EDR transmit power within Class 2 or Class 3 designs and should be set to 0 for all power table entries.

4.2 Class 1 Power Table Configuration

CSR recommends using firmware build Unified21a or later for Class 1 designs that support the Bluetooth version 2.0 + EDR specification. Power table configuration for this type of design is described in section 3.

HCIStack2.0EDRv19.2 can be used in Class 1 designs. However, configuration options are restricted due to the limited functionality of the EDR and EXT PA control bits. The control bits are jointly used to enable dynamic switching of an external PA and to limit EDR transmissions with an external PA. These functions cannot be configured independently of one another, as is done in later versions of firmware.

If the design does not use dynamic switching of an external PA, then all control bits should be set to 0. EDR transmit power can be restricted by repeating the maximum EDR power setting for all higher Basic Rate power table entries. The Basic Rate EXT PA and EDR EXT PA gain settings control the AUX_DAC during Basic Rate and EDR transmissions if PSKEY_TXRXPIO_CONTROL is configured to use the AUX_DAC for gain control of an external PA.

If the design uses dynamic switching of the external PA, then both the EXT PA and EDR control bits must be set to 1 for all high-power entries using the external PA. This invokes the following functionality for high-power transmissions:

- PIO[1] is pulled high (if functionality is set in PSKEY_TXRXPIO_CONTROL).
- The PIO given by PSKEY_TX_AVOID_PA_CLASS1PIO is de-asserted.
- EDR transmit power is limited either by renegotiating the link to Basic Rate operation (LIMIT_EDR_POWER disabled) or by refusing to increase power to high-power entries (LIMIT_EDR_POWER enabled).
- Class 1-specific PS keys are enabled.

For low-power transmissions, both EXT PA and EDR control bits are set to 0 and device functionality changes as follows:

- PIO[1] is pulled low.
- The PIO given by PSKEY_TX_AVOID_PA_CLASS1_PIO is asserted.
- BlueCore uses the default PS key settings (e.g. PSKEY_TX_PRE_LVL and PSKEY_TRANSMIT_OFFSET_HALF_MHZ.)
Related PS Keys

This section gives a summary of PS keys that rely on the power table and that typically need to be configured on a per-design basis. Specific documentation for each of these keys is provided with each BlueCore build and it is intended and expected that the reader will refer to that for the latest documentation. By its nature, this overview document cannot reflect small changes that may occur between firmware builds, or may have occurred after this document was published.

In case of discrepancy between this document and the documentation supplied with each firmware build, the latter should be regarded as definitive.

5.1 PSKEY_LC_MAX_TX_POWER (0x017)

This key defines the maximum power (in dBm) at which the device can transmit. The power table serves as a lookup table that the LMP uses to associate the value given by PSKEY_LC_MAX_TX_POWER with the required amplifier drive settings. The firmware uses the highest value in the power table that is less than or equal to the requested power. Any entries that have a higher transmit power than this key are ignored. If this key is set below the lowest entry in the power table, then BlueCore behaves as if the power table contained just its first row, even though that power is higher than the stated maximum power. This is a fail-safe feature.

EDR transmissions can be limited to a power level below this setting through the use of the EDR control bit, as described in section 3.1.

PSKEY_LC_MAX_TX_POWER should not exceed the maximum transmit power for the class limits of the device (0dBm for Class 3, +4dBm for Class 2 and +20dBm for Class 1) or for which the design obtains Bluetooth qualification.

5.2 PSKEY_LC_DEFAULT_TX_POWER (0x021)

This key defines the transmit power (in dBm) at which BlueCore performs page and inquiry functions, their scan responses and new connections. If the value of this key does not exactly match an entry in the power table, BlueCore uses the highest value in the power table that is less than or equal to the requested default power.

For high-power Class 1 devices, higher values assist with the discovery and connection to devices located far away (>10m), but may create problems connecting to close-in devices due to receiver saturation. Conversely, lower values reduce the possibility of receiver saturation in a remote device but could create problems with the discovery of and connection to far away devices. Applications may overcome this limitation by using BCCMD commands to dynamically override this PS key in order to conduct inquiry and paging at both high (e.g. +20dBm) and low (e.g. +4dBm) transmit powers.

5.3 PSKEY_LC_MAX_TX_POWER_NO_RSSI (0x02d)

The Bluetooth specification requires that Class 1 devices limit transmit power to a maximum of +4dBm if the receiving device does not support power control. PSKEY_LC_MAX_TX_POWER_NO_RSSI gives the maximum transmit power used by BlueCore if the receiving device does not support power control messaging. For a Class 1 design, this value must not exceed +4dBm. For Class 2 and Class 3 designs, this key should be set to the same value as PSKEY_LC_DEFAULT_TX_POWER.

5.4 PSKEY_LOCAL_SUPPORTED_FEATURES (0xef)

This key enables or disables EDR capabilities in BlueCore4 chips. The default setting in Unified21a firmware (which enables EDR) is 0xffff 0xfe8f 0xf99b 0x8000.

The setting for disabling EDR is 0xffff 0xf88f 0x1818 0x8000.
5.5 PSKEY_TXRXPIO_CONTROL (0x209)

This key configures the RF front-end (PA/LNA/switch) control signalling using PIO[1], PIO[0] and the AUX_DAC. The control signalling options are:

- 0: PIO[0] and PIO[1] are not driven for RX and TX modes. TX power ramping is controlled by the internal PA.
- 1: PIO[0] and PIO[1] are driven high for RX and TX modes respectively. TX power ramping is controlled by the internal PA.
- 2: PIO[0] and PIO[1] are driven high for RX and TX modes respectively. The AUX_DAC is used for TX power ramping and gain control of an external PA if the EDR control bit is disabled.
- 3: PIO[0] and PIO[1] are driven low for RX and TX modes respectively. TX power ramping is controlled by the internal PA.
- 4: PIO[0] and PIO[1] are driven high for RX and TX modes respectively. The internal PA is used for TX power ramping. AUX_DAC is used for gain control of an external PA if the EDR control bit is disabled.
- 5: PIO[0] and PIO[1] are driven high for RX and TX modes respectively. The internal PA is used for TX power ramping. AUX_DAC is used for gain control of an external LNA.

5.6 PSKEY_TX_AVOID_PA_CLASS1PIO (0x3b3)

For a design with non-zero EXT PA control bits in PSKEY_LC_ENHANCED_POWER_TABLE, this key defines the PIO that is asserted for transmissions with the EXT PA control bit set to 0. This feature is typically used to implement a switchable external PA.

A key value of 1 is not allowed because PIO[1] is required to enable/disable the external PA. A key value of greater than 15 indicates that no PIO is asserted when the external PA is not in use. If a device is not configured for operation with a switchable external PA (i.e. all EXT PA settings are set to 0) then this PS key is ignored.

5.7 PSKEY_TRANSMIT_OFFSET_CLASS1 (0x3b4)

For a design with non-zero EXT PA control bits in PSKEY_LC_ENHANCED_POWER_TABLE, this key defines the transmit offset, in units of 62.5 kHz, used for transmissions with the EXT PA control bit set to 1. Entries with the EXT PA control bit set to 0 use PSKEY_TX_PRE_LVL_HALF_MHZ (or PSKEY_TRANSMIT_OFFSET_HALF_MHZ, if applicable). This allows for separate Class 1 and Class 2 configuration of the transmit offset in designs using a switchable external PA.

5.8 PSKEY_TX_PRE_LVL_CLASS1 (0x3a8)

For a design with non-zero EXT PA control bits in PSKEY_LC_ENHANCED_POWER_TABLE, this key sets the level of the internal pre-amplifier used for transmissions with the EXT PA control bit set to 1. Entries with the EXT PA control bit set to 0 use PSKEY_TX_PRE_LVL. This allows for separate Class 1 and Class 2 configuration of the pre-amplifier gain in designs using a switchable external PA.
## Document References

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<td>n/a</td>
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<td>Transmit Power Control</td>
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### Terms and Definitions

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BlueCore™

Enhanced Power Table Construction

Application Note

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